## IN THE CLAIMS

1. (original) A bonding pad for an integrated circuit, the bonding pad comprising:

a conductive base layer having slots formed therein, the slots extending completely through the conductive base layer,

an insulating layer disposed on top of the conductive base layer, the insulating layer protruding into the slots of the conductive base layer, and the insulating layer including a low k material, and

a conductive top layer disposed on top of the insulating layer, where the conductive base layer and the conductive top layer are not directly physically contacting one another.

2. (original) The bonding pad of claim 1 further comprising a plurality of vias extending through the insulating layer and electrically connecting the conductive base layer to the conductive top layer at peripheral portions of the conductive base layer and the conductive top layer.

3. (original) The bonding pad of claim 1 wherein the insulating layer comprises a base oxide layer on top of the conductive base layer, a low k dielectric layer on top of the base oxide layer, and a cap oxide layer between the low k dielectric layer and the conductive top layer.

4. (original) The bonding pad of claim 1 wherein both the conductive base layer and the conductive top layer comprise a metal selected from the group consisting of aluminum, copper, nickel, ruthenium, titanium, tungsten, platinum, and gold.

5. (original) The bonding pad of claim 1 wherein the slots of the conductive base layer comprise a pattern of substantially parallel slots.

6. (original) The bonding pad of claim 1 wherein the slots of the conductive base layer have a width of about eleven microns and a spacing of about three microns.

7. (original) The bonding pad of claim 1 wherein the insulating layer has a thickness measured between the conductive base layer and the conductive top layer of from about three thousand angstroms to about fifteen thousand angstroms.

8. (original) The bonding pad of claim 1 further comprising multiple layers of the conductive base layer and the overlying insulating layer below the conductive top layer.

9. (original) An integrated circuit, the improvement comprising the bonding pad of claim 1.

10. (cancelled)
11. (cancelled)
12. (cancelled)
13. (cancelled)
14. (cancelled)
15. (cancelled)
16. (cancelled)
17. (cancelled)
18. (cancelled)

19. (original) An integrated circuit, the improvement comprising a bonding pad having:

a conductive base layer having slots formed therein, the slots extending completely through the conductive base layer,

an insulating layer disposed on top of the conductive base layer, the insulating layer protruding into the slots of the conductive base layer, and the insulating layer including a low k material, and

a conductive top layer disposed on top of the insulating layer, where the conductive base layer and the conductive top layer are not directly physically contacting one another.

20. (original) The integrated circuit of claim 19 wherein the insulating layer comprises a base oxide layer on top of the conductive base layer, a low k

dielectric layer on top of the base oxide layer, and a cap oxide layer between the low k dielectric layer and the conductive top layer.

21. (original) The integrated circuit of claim 19 wherein the slots of the conductive base layer have a width of about eleven microns and a spacing of about three microns.

22. (original) The integrated circuit of claim 19 wherein the insulating layer has a thickness measured between the conductive base layer and the conductive top layer of from about three thousand angstroms to about fifteen thousand angstroms.

23. (original) The integrated circuit of claim 19 further comprising multiple layers of the conductive base layer and the overlying insulating layer below the conductive top layer.